Electronic Version
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Claims

[c1] 1.A divide-by-X.5 circuit, wherein X is a whole number, comprising:

a phase-locked loop having a voltage-controlled oscillator (VCO) that generates four phase clocks having a same input frequency but having differing phase offsets;

a first divide-by-X-plus-two circuit, receiving a first phase clock of the four phase clocks, for generating a first divided-by-X-plus-two signal that has a frequency being the input frequency divided by (X+2), the first divided-by-X-plus-two signal being synchronous to the first phase clock;

a second divide-by-X-plus-two circuit, wherein X-plus-two is twice X, receiving a second phase clock of the four phase clocks, for generating a second divided-by-X-plus-two signal that has a frequency being the input frequency divided by (X+2), the second divided-by-X-plus-two signal being synchronous to the second phase clock;

a third divide-by-X-plus-two circuit, wherein X-plus-two is twice X, receiving a third phase clock of the four phase clocks, for generating a third divided-by-X-plus-two signal that has a frequency being the in-

put frequency divided by (X+2), the third divided-by-X-plus-two signal being synchronous to the third phase clock;

a fourth divide-by-X-plus-two circuit, wherein X-plus-two is twice X, receiving a fourth phase clock of the four phase clocks, for generating a fourth divided-by-X-plus-two signal that has a frequency being the input frequency divided by (X+2), the fourth divided-by-X-plus-two signal being synchronous to the fourth phase clock; and

a frequency doubler, receiving the first, second, third, and fourth divided-by-X-plus-two signals, for generating an output clock having an output frequency that is the input frequency divided by X.5,

whereby the output clock is generated from the four phase clocks from the voltage-controlled oscillator.

[c2] 2.The divide-by-X.5 circuit of claim 1 wherein the frequency doubler comprises:

a first gate, receiving the first divided-by-X-plus-two signal and the fourth divided-by-X-plus-two signal;

a second gate, receiving the second divided-by-X-plus-two signal and the third divided-by-X-plus-two signal;

a summing gate, coupled to the first and second gates, for generating the output clock.

[c3] 3.The divide-by-X.5 circuit of claim 2 wherein the first gate, the second gate, and the summing gate are NAND gates.

[c4] 4.The divide-by-X.5 circuit of claim 3 further comprising:
a reset sequencer, receiving a system reset signal, for generating a sequence of staggered reset signals applied to the first, second, third, and fourth divide-by-X-plus-two circuit to successively activate the first, second, third, and fourth divide-by-X-plus-two circuits upon completion of reset.

[c5] 5.The divide-by-X.5 circuit of claim 4 wherein the reset sequencer comprises:
a first flip-flop receiving the system reset signal and generating a first reset to the first divide-by-X-plus-two circuit;
a second flip-flop receiving an output of the first flip-flop and generating a second reset to the second divide-by-X-plus-two circuit;
a third flip-flop receiving an output of the second flip-flop and generating a third reset to the third divide-by-X-plus-two circuit; and
a fourth flip-flop receiving an output of the third flip-flop and generating a fourth reset to the fourth divide-

by-X-plus-two circuit.

[c6] 6.The divide-by-X.5 circuit of claim 5 wherein the first flip-flop is clocked by the first phase clock;
wherein the second flip-flop is clocked by the second phase clock;
wherein the third flip-flop is clocked by the third phase clock;
wherein the fourth flip-flop is clocked by the fourth phase clock,
whereby flip-flops are clocked by different phases.

[c7] 7.The divide-by-X.5 circuit of claim 2 wherein the voltage-controlled oscillator comprises:
a first differential stage receiving a first true input and a first complement input and generating a first true output and a first complement output;
a second differential stage receiving the first true output and the first complement output and generating a second true output and a second complement output;
a third differential stage receiving the second true output and the second complement output and generating a third true output and a third complement output;
a fourth differential stage receiving the third true output and the third complement output and generating a fourth true output and a fourth complement output;
wherein the fourth true output is applied to the first

complement input of the first differential stage;
wherein the fourth complement output is applied to the first true input of the first differential stage.

[c8] 8.The divide-by-X.5 circuit of claim 7 further comprising:
differential to single-ended converters, each receiving a pair of true and complement outputs from the first, second, third, or fourth differential stages, for generating the four phase clocks.

[c9] 9.The divide-by-X.5 circuit of claim 8 wherein the voltage-controlled oscillator generates quadrature phases for the four phase clocks, the four phase clocks having phases offsets that are multiplies of about 90 degrees.

[c10] 10.The divide-by-X.5 circuit of claim 9 wherein the second phase clock has a phase of about 270 degrees relative to the first phase clock;
wherein the third phase clock has a phase of about 180 degrees relative to the first phase clock;
wherein the fourth phase clock has a phase of about 90 degrees relative to the first phase clock.

[c11] 11.The divide-by-X.5 circuit of claim 10 wherein X is 1 and X-plus-two is 3,
wherein the divide-by-X.5 circuit divides the input fre-

quency by 1.5 to generate the output frequency.

[c12] 12.A divider comprising:

quadrature clock means for generating a first clock, a second clock, a third clock, and a fourth clock all having an input frequency but having differing phases;

first double divider means, receiving the first clock, for generating a first divided clock having an intermediate frequency that is the input frequency divided by X+2;

wherein X is an odd integer greater than zero;

second double divider means, receiving the second clock, for generating a second divided clock having the intermediate frequency that is the input frequency divided by X+2;

third double divider means, receiving the third clock, for generating a third divided clock having the intermediate frequency that is the input frequency divided by X+2;

fourth double divider means, receiving the fourth clock, for generating a fourth divided clock having the intermediate frequency that is the input frequency divided by X+2;

reset sequence means, receiving the first, second, third, and fourth clocks, for generating a first reset signal to the first double divider means, a second reset signal to the second double divider means, a third reset signal to the third double divider means, and a fourth reset signal

to the fourth double divider means, the reset sequence means de-activating the first, second, third, and fourth reset signals at separate times in a sequence; and

frequency doubling means, receiving the first, second, third, and fourth divided clocks, for generating an output clock having an output frequency that is double am intermediate frequency of the first divided clock,

whereby the input frequency is X.5 times the output frequency.

[c13] 13.The divider of claim 12 wherein the second clock has a phase of about 270 degrees relative to the first clock;

wherein the third clock has a phase of about 180 degrees relative to the first clock;

wherein the fourth clock has a phase of about 90 degrees relative to the first clock.

[c14] 14.The divider of claim 13 wherein X is one.

[c15] 15.The divider of claim 13 further comprising:

phase compare means, receiving a reference clock and a feedback clock, for comparing phases of the feedback clock to the reference clock;

loop filter means for generating a control voltage;

charge pump means, responsive to the phase compare means, for charging and discharging the loop filter means;

wherein the quadrature clock means is part of a voltage-controlled oscillator that receives the control voltage from the loop filter means, the voltage-controlled oscillator also generating the feedback clock or a pre-feedback clock.

[c16] 16.The divider of claim 15 further comprising:
feedback divider means, receiving the pre-feedback clock from the voltage-controlled oscillator, for generating the feedback clock by dividing the pre-feedback clock.

[c17] 17.The divider of claim 16 further comprising:
differential convert means, receiving differential pairs of oscillator clocks from the voltage-controlled oscillator, for generating the first, second, third, and fourth clocks from the differential pairs of oscillator clocks.

[c18] 18.A 1.5 divider comprising:
a phase-locked loop with a voltage-controlled oscillator that generates a first clock having a first phase, a second clock having a second phase that is offset from the first phase, a third clock having a third phase that is offset from the first phase and from the second phase, and a fourth clock having a fourth phase that is offset from the first phase, the second phase, and the third phase;
a reset generator, receiving a master reset signal, for

generating a first reset signal, a second reset signal, a third reset signal, and a fourth reset signal that are deactivated with differing delays from the master reset signal;

a first divider, clocked by the first clock, and activated by the first reset signal, generating a first divided clock, the first divider having an odd positive divisor;

a second divider, clocked by the second clock, and activated by the second reset signal, generating a second divided clock, the second divider having the odd positive divisor;

a third divider, clocked by the third clock, and activated by the third reset signal, generating a third divided clock, the third divider having the odd positive divisor;

a fourth divider, clocked by the fourth clock, and activated by the fourth reset signal, generating a fourth divided clock, the fourth divider having the odd positive divisor;

a frequency doubler, receiving the first, second, third, and fourth divided clocks, for generating an output clock by logically combining the first, second, third, and fourth divided clocks, the output clock having a frequency that is double a frequency of the first divided clock.

[c19] 19.The 1.5 divider of claim 18 wherein the odd positive divisor is 3, wherein the output clock has a frequency

that is a factor of 1.5 less than an input frequency of the first clock.

[c20] 20.The 1.5 divider of claim 18 wherein the frequency doubler comprises:

a first NAND gate, receiving the first divided clock and the fourth divided clock;

a second NAND gate, receiving the second divided clock and the third divided clock;

a summing gate, coupled to the first and second NAND gates, for generating the output clock.